WHAT IS CLAIMED IS:

1. A wiring substrate characterized in comprising:

a wiring layer formed on a substrate; and

terminal electrodes that are connected to the wiring layer and disposed based on a stress distribution that works on the substrate.

2. A wiring substrate characterized in comprising:

a wiring layer formed on a substrate; and

terminal electrodes that are connected to the wiring layer and disposed on the substrate in a manner to avoid diagonal lines thereof.

3. A wiring substrate characterized in comprising:

a wiring layer formed on a substrate;

terminal electrodes that are connected to the wiring layer and disposed on the substrate; and

stress insulation sections provided along diagonal lines of the substrate.

4. A wiring substrate according to claim 3, characterized in that the stress insulation sections are at least one of grooves and slits.

5. A wiring substrate characterized in comprising:

a wiring layer formed on a substrate;

terminal electrodes that are connected to the wiring layer and disposed on the substrate; and

dummy terminals provided in four corners or on diagonal lines of the substrate.

6. A semiconductor device characterized in comprising:

a semiconductor chip having an active region and pad electrodes formed thereon;

a stress buffer layer formed on the active region;

bump electrodes that are formed on the stress buffer layer and disposed based on a stress distribution that works on the semiconductor chip;

rearrangement wiring layers that connect the bump electrodes and the pad electrodes; and

a protection layer that is formed over the rearrangement wiring layers and the pad electrodes.

7. A semiconductor device characterized in comprising:

a semiconductor chip having an active region and pad electrodes formed thereon;

a stress buffer layer formed on the active region;

bump electrodes that are formed on the stress buffer layer and disposed in a manner to avoid diagonal lines thereof;

rearrangement wiring layers that connect the bump electrodes and the pad electrodes; and

a protection layer that is formed over the rearrangement wiring layers and the pad electrodes.

8. A semiconductor device characterized in comprising:

a semiconductor chip having an active region and pad electrodes formed thereon;

stress buffer layers that are formed on the active region, and divided and disposed along diagonal lines;

bump electrodes formed on the stress buffer layers;

rearrangement wiring layers that connect the bump electrodes and the pad electrodes; and

protection layers that are formed over the rearrangement wiring layers and the pad electrodes, and divided and disposed along the diagonal lines.

9. A semiconductor device characterized in comprising:

a semiconductor chip having an active region and pad electrodes formed thereon;

a stress buffer layer that is formed on the active region;

bump electrodes formed on the stress buffer layer;

dummy bumps provided in four corners or on diagonal lines of the stress buffer layer;

rearrangement wiring layers that connect the bump electrodes and the pad electrodes; and

a protection layer that is formed over the rearrangement wiring layers and the pad electrodes.

10. A semiconductor module characterized in comprising:

an interposer substrate having a semiconductor chip surface-mounted thereon;

a wiring layer provided on a back surface of the interposer substrate;

bump electrodes that are connected to the wiring layer and disposed based on a stress distribution that works on the interposer substrate; and

through hole wirings that are provided in the interposer substrate and connect the semiconductor chip and the wiring layer.

11. A semiconductor module characterized in comprising:

an interposer substrate having a semiconductor chip surface-mounted thereon;

a wiring layer provided on a back surface of the interposer substrate;

bump electrodes that are connected to the wiring layer and disposed on the back surface of the interposer substrate in a manner to avoid diagonal lines; and

through hole wirings that are provided in the interposer substrate and connect the semiconductor chip and the wiring layer.

12. A semiconductor module characterized in comprising:

an interposer substrate having a semiconductor chip surface-mounted thereon;

a wiring layer provided on a back surface of the interposer substrate;

bump electrodes that are connected to the wiring layer and disposed on the back surface of the interposer substrate in a manner to avoid diagonal lines;

at least one of grooves and slits provided along diagonal lines of the interposer substrate; and

through hole wirings that are provided in the interposer substrate and connect the semiconductor chip and the wiring layer.

13. A semiconductor module characterized in comprising:

an interposer substrate having a semiconductor chip surface-mounted thereon;

a wiring layer provided on a back surface of the interposer substrate;

bump electrodes that are connected to the wiring layer and disposed on the back surface of the interposer substrate;

dummy bumps provided in four corners or on diagonal lines of the back surface of the interposer substrate; and

through hole wirings that are provided in the interposer substrate and connect the semiconductor chip and the wiring layer.

14. An electronic device characterized in comprising:

an interposer substrate having a semiconductor chip surface-mounted thereon;

a wiring layer provided on a back surface of the interposer substrate;

bump electrodes that are connected to the wiring layer and disposed on the back surface of the interposer substrate in a manner to avoid diagonal lines;

through hole wirings that are provided in the interposer substrate and connect the semiconductor chip and the wiring layer;

a mother substrate having the interposer substrate mounted thereon; and

an electronic component that is connected to the bump electrodes through the mother substrate.

15. A method for designing a wiring substrate, characterized in that, based on a stress distribution that works on a wiring substrate, disposing positions of bump electrodes on the wiring substrate are determined.

16. A method for designing a wiring substrate according to claim 15, characterized in that the disposing positions of the bump electrodes on the wiring substrate are determined in a manner to avoid diagonal lines of the wiring substrate.

17. A method for manufacturing a semiconductor device, characterized in comprising:

a step of forming a stress buffer layer on an active region of a semiconductor chip having pad electrodes formed thereon;

a step of exposing the pad electrodes by patterning the stress buffer layer;

a step of forming rearrangement wiring layers that extend from the pad electrodes over the stress buffer layer;

a step of forming a protection layer over the rearrangement wiring layers;

a step of forming opening sections that expose the rearrangement wiring layers in a manner to avoid diagonal line by patterning the protection layer; and

a step of forming, on the stress buffer layer, bump electrodes that are connected to the rearrangement wiring layers through the opening sections.

18. A method for manufacturing a semiconductor device, characterized in comprising:

a step of forming a stress buffer layer on an active region of a semiconductor chip having pad electrodes formed thereon;

a step of dividing the stress buffer layer along diagonal lines and exposing the pad electrodes by patterning the stress buffer layer;

a step of forming rearrangement wiring layers that extend from the pad electrodes over the stress buffer layer;

a step of forming a protection layer over the rearrangement wiring layers;

a step of forming opening sections that divide the protection layer along the diagonal lines and expose the rearrangement wiring layers by patterning the protection layer; and

a step of forming, on the stress buffer layer, bump electrodes that are connected to the rearrangement wiring layers through the opening sections.

19. A method for manufacturing a semiconductor device, characterized in comprising:

a step of forming a stress buffer layer on an active region of a semiconductor chip having pad electrodes formed thereon;

a step of exposing the pad electrodes by patterning the stress buffer layer;

a step of forming rearrangement wiring layers that extend from the pad electrodes over the stress buffer layer, and dummy lands in four corners or on diagonal lines on the stress buffer layer:

a step of forming a protection layer over the rearrangement wiring layers and the dummy lands;

a step of forming, by patterning the protection layer, first opening sections that expose the rearrangement wiring layers and second opening sections that expose the dummy lands; and

a step of forming, on the stress buffer layer, bump electrodes that are connected to the rearrangement wiring layers through the first opening sections, and forming dummy bumps disposed over the dummy lands through the second opening sections.

20. A method for manufacturing a semiconductor module, characterized in comprising:

a step of forming wiring layers connected via through holes on both sides of an interposer substrate;

a step of forming bump electrodes connected to the wiring layer on a back surface of the interposer substrate in a manner to avoid diagonal lines; and

a step of mounting a semiconductor chip on a front surface of the interposer substrate.

21. A method for manufacturing a semiconductor module, characterized in comprising:

a step of forming at least one of grooves and slits along diagonal lines of an interposer substrate;

a step of forming wiring layers connected via through holes on both sides of the interposer substrate;

a step of forming bump electrodes connected to the wiring layer on a back surface of the interposer substrate; and

a step of mounting a semiconductor chip on a front surface of the interposer substrate.

22. A method for manufacturing a semiconductor module, characterized in comprising:

a step of forming wiring layers connected via through holes on both sides of the interposer substrate, and forming dummy lands in four corners or on diagonal lines of a back surface of the interposer substrate;

a step of forming bump electrodes connected to the wiring layer on the back surface of the interposer substrate, and forming dummy bumps on the dummy lands; and

a step of mounting a semiconductor chip on a front surface of the interposer substrate.